

**Application No.: 10/813,062****Docket No.: 4459-144****AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (original) A package structure with a cavity comprising:  
a chip having a circuit disposed thereon and a plurality of first bonding pads disposed around the circuit, and the first bonding pads electrically connected to the circuit and an external circuit;  
a multi-layer ceramic substrate having a cave formed thereon and a plurality of second bonding pads disposed around the cave, wherein the cave and the plurality of second bonding pads are corresponding to the circuit and the plurality of first bonding pads, respectively; and  
an adhesive layer being substantially applied to the surface of the substrate, with the cave and the second bonding pads exposed from the adhesive layer, for tightly bonding the chip and the multi-layer ceramic substrate together such that the circuit of the chip is corresponding to the cave of the multi-layer ceramic substrate so as to form a cavity;  
wherein the plurality of second bonding pads are respectively connected to a plurality of via conductors on the multi-layer ceramic substrate so as to connect with an external circuit.
2. (original) The package structure with a cavity as claimed in claim 1, wherein the chip is a SAW chip, and the circuit is an interdigital transducer (IDT).
3. (original) The package structure with a cavity as claimed in claim 1, wherein the chip is a semiconductor chip.

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4. (original) The package structure with a cavity as claimed in claim 1, wherein the chip is an optical chip.
5. (original) The package structure with a cavity as claimed in claim 1, wherein the chip is a crystal chip.
6. (original) The package structure with a cavity as claimed in claim 1, wherein the chip is a MEMS chip.
7. (original) The package structure with a cavity as claimed in claim 1, wherein the material of the multi-layer ceramic substrate is selected from a group of AlN, low-temperature co-fired ceramic (LTCC), multi-layer co-fired ceramic (MLCC), AL.sub.2O.sub.3, and polymeric materials.
8. (original) The package structure with a cavity as claimed in claim 1, wherein the plurality of first bonding pads are electrically connected to the plurality of second bonding pads by a gold layer.
9. (original) The package structure with a cavity as claimed in claim 1 further comprising a buffer resin sealing and protecting the upper portion of the chip and the multi-layer ceramic substrate for stress relaxation and electrical insulation.
10. (original) The package structure with a cavity as claimed in claim 9 further comprising a epoxy resin sealing and protecting the buffer resin for mechanical protection and enhancement of moisture resistance.
11. (new) The package structure with a cavity as claimed in claim 1, wherein the

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multi-layer ceramic substrate has a plurality of via conductors formed thereon for electrically connecting the plurality of second bonding pads and an external circuit.

12. (new) A package structure with a cavity comprising:

a SAW chip having a first surface, a second surface opposite to the first surface, an interdigital transducer (IDT) disposed on the first surface, and a plurality of first bonding pads disposed around the interdigital transducer on the first surface;

a multi-layer ceramic substrate having a cave formed thereon and a plurality of second bonding pads disposed around the cave and electrically connected to the first bonding pads, wherein the cave and the plurality of second bonding pads are corresponding to the interdigital transducer and the plurality of first bonding pads, respectively; and

an adhesive layer formed around the cave and between the first surface of the SAW chip and the multi-layer ceramic substrate for tightly bonding the SAW chip and the multi-layer ceramic substrate together, wherein the first surface of the SAW chip, the adhesive layer and the cave of the multi-layer ceramic substrate together define a cavity such that the interdigital transducer of the SAW chip is disposed within the cavity.

13. (new) The package structure as claimed in claim 11, wherein the multi-layer ceramic substrate has a plurality of via conductors formed thereon for electrically connecting the plurality of second bonding pads and an external circuit.

14. (new) The package structure as claimed in claim 11, wherein the material of the multi-layer ceramic substrate is selected from a group of AlN, low-temperature co-fired ceramic (LTCC), multi-layer co-fired ceramic (MLCC), AL<sub>2</sub>O<sub>3</sub>, and polymeric materials.

15. (new) The package structure as claimed in claim 11, wherein the plurality of first bonding pads are electrically connected to the plurality of second bonding pads by a gold layer.

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16. (new) The package structure as claimed in claim 11, further comprising a buffer resin sealing and protecting the upper portion of the chip and the multi-layer ceramic substrate for stress relaxation and electrical insulation.

17. (new) The package structure as claimed in claim 16, further comprising a epoxy resin sealing and protecting the buffer resin for mechanical protection and enhancement of moisture resistance.

18. (new) The package structure of claim 1, wherein said cavity is free of said adhesive layer which directly and hermetically bonds said chip and said substrate together.

19. (new) The package structure of claim 1, wherein said cavity is free of said adhesive layer and said second bonding pads are spaced from a circumference of said cavity by said adhesive layer.

20. (new) The package structure of claim 19, wherein said cavity is free of said adhesive layer and said bonding pads are spaced from each other by said adhesive layer.